

REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Non-Final Office Action of December 3, 2004 has been received and its contents carefully reviewed.

Claims 1-26 are currently pending in the present application. Reexamination and reconsideration of the pending claims is respectfully requested.

In the Office Action, the Examiner rejected claims 1-26 under 35 U.S.C. §103(a) as being unpatentable over Moon et al. (U.S. Patent No. 5,793,346) in view of Tsuchi et al. (U.S. Patent No. 5,818,406). Applicants respectfully traverse this rejection.

Claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, "...level shifting means for receiving a power supply voltage and a ground voltage... to apply a higher voltage level than the ground voltage to the gate lines upon power-off." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention.

In the Office Action on page 3, the Examiner admits that Moon et al. fails to teach the aforementioned feature recited in claim 1. Then, in order to cure the deficiencies of Moon et al., the Examiner cites Tsuchi et al. as teaching the aforementioned feature in claim 1, stating "Tsuchi teaches a driver circuit for a LCD device... teaches how a higher voltage level than ground voltage (i.e., 5V) is applied to the transistors upon power-off (column 8, lines 14-35, figures 9-12)." Applicants respectfully disagrees. Tsuchi et al. does not supply the deficiencies of Moon et al. with respect to claim 1.

Fig. 12 of Tsuchi et al. is "a circuit diagram showing an internal construction of the functional block 50 in the driver circuit of Fig. 7." Further, Tsuchi et al. at Col. 8, lines 14-35 (Examiner's citation) discloses, "...signals are converted from low voltage system (5V) to high voltage system (18V) by the level shifter 71, and taken out through a line 67."

As shown in Fig. 12 of Tsuchi et al., the low voltage system (5V) the Examiner refers to is converted to the high voltage system (18V) by a level shifter, and then it is sent to the data lines through the semiconductor switches. In contrast to Tsuchi et al., a voltage level higher than the ground voltage is applied to *the gate lines* in the present application when the power is

turned off, as recited in claim 1. [emphasis added]. Further, nowhere does Tsuchi et al. disclose that 5V (Examiner's citation) is applied when the power of the LCD is turned off. Accordingly, Applicants respectfully submit that claim 1 and claims 2-8, which depend therefrom, are allowable over the cited references.

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, "... applying a higher level voltage than the ground voltage to the gate lines upon power-off." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Applicants respectfully submit that claim 9 and claim 10, which depends therefrom, are allowable over the cited references.

Claim 11 is allowable over the cited references in that claim 11 recites a combination of elements including, for example, "...when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Applicants respectfully submit that claim 11 and claims 12-18, which depend therefrom, are allowable over the cited references.

It appears that the Examiner cites Moon et al. as teaching the aforementioned feature recited in claim 11. Applicants respectfully disagree. The Examiner's attention is directed to the bottom graph of Fig. 5 in Moon et al. As shown, when the power is turned off ("T"), the voltage at node N2, which is the output of the screen clearing circuit 40, approaches the ground voltage ("GND").

Claim 19 is allowable over the cited references in that claim 19 recites a combination of elements including, for example, "...when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Applicants respectfully submit that claim 19 and claims 20-26, which depend therefrom, are allowable over the cited references.

Applicants believe the application is in condition for allowance and early, favorable action is respectfully solicited. If the Examiner deems that a telephone conversation would

further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

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